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Dirac point and transconductance of top-gated graphene field-effect transistors operating at elevated temperature

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Top-gated graphene field-effect transistors (GFETs) have been fabricated using bilayer epitaxial graphene grown on the Si-face of 4H-SiC substrates by thermal decomposition of silicon carbide in high vacuum. Graphene films were characterized by Raman spectroscopy, Atomic Force Microscopy, Scanning Tunnelling Microscopy, and Hall measurements to estimate graphene thickness, morphology, and charge transport properties. A 27 nm thick Al_2O_3 gate dielectric was grown by atomic layer deposition with an e-beam evaporated Al seed layer. Electrical characterization of the GFETs has been performed at operating temperatures up to 100 °C limited by deterioration of the gate dielectric performance at higher temperatures. Devices displayed stable operation with the gate oxide dielectric strength exceeding 4.5 MV/cm at 100 °C. Significant shifting of the charge neutrality point and an increase of the peak transconductance were observed in the GFETs as the operating temperature was elevated from room temperature to 100 °C. © *2014 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4898562]

I. INTRODUCTION

Graphene is a single atomic plane of graphite, with unique and superior physical properties resulting from its purely two-dimensional nature.[1] The extremely high carrier mobility and surface carrier density in graphene make it an exceptional material choice for the development of new generations of electronic devices. Indeed, top-gated graphene field-effect transistors (GFETs) with a peak extrinsic transconductance (g_m) exceeding 600 mS/mm and current density more than 3 A/mm have been demonstrated[2,3] on epitaxial graphene (EG) grown by thermal decomposition of silicon carbide (SiC)[4] allowing wafer scale production of graphene devices. While monolayer graphene is a zero band gap material, it was theoretically predicted that a band gap may be induced in bilayer graphene by a perpendicular electric field[5] and GFETs with on/off ratios corresponding to a band gap of about 100 mV were demonstrated on epitaxial[6] and exfoliated[7] bilayer graphene. In addition, GFETs demonstrate unique ambipolar characteristics, when the channel conductivity type changes with applied gate voltage about the Dirac charge neutrality point (V_{CNP}). If the exceptional thermal stability and superior thermal conductivity of graphene[1] is also taken into account, GFETs may be considered as promising building blocks for development of high frequency analogue electronics including, for example, frequency multipliers, mixers, and oscillators. In order to realize these potential applications, which would require operation of the devices at elevated temperatures it is critical to know the change of GFET parameters with increasing temperature. In particular, these parameters include transconductance (g_m), which determines the amplifying ability of GFETs and the Dirac point voltage, which defines the required dc bias at the working point. Nevertheless, the temperature dependence of GFET characteristics and charge carrier transport in graphene has barely been addressed up to now. It was found that carrier mobility in exfoliated monolayer graphene decreases with increasing temperature in the range of 2–350 K due to scattering by thermally excited polar surface phonons in the SiO_2 substrate.[8] Similar decrease of carrier mobility with increasing temperature from 110 to 300 K was observed in single-layer EG grown on the Si-face of SiC and covered by an Al_2O_3 gate dielectric grown by atomic layer deposition (ALD).[9] As long as the g_m value is directly proportional to the carrier mobility for a long-channel FET in its linear working region,[10] the peak transconductance of a GFET has to follow the same temperature dependence as carrier mobility. Indeed, a decrease in the peak transconductance was observed in top-gated GFETs made of exfoliated graphene with polymer NFC/HfO_2 top-gate dielectric when the temperature was changed from 5 to 300 K.[11] In bilayer and tri-layer exfoliated graphene, however, the charge carrier mobility increases with temperature due to dominant Coulomb scattering for these graphenes.[8] This has to result in different temperature behaviour of bilayer and trilayer GFETs, namely, in an increase of peak transconductance with temperature although it may be hidden by the effect of a top gate insulator and the SiC substrate in EG. To the best of our knowledge, no work has yet been done to investigate the temperature dependence of the electrical characteristics of GFETs made of bilayer graphene, in particular under elevated temperature conditions (i.e., above room temperature). This paper reports on the fabrication of GFETs using bilayer EG grown on SiC substrates and an ALD-grown Al_2O_3

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top-gate dielectric and presents their electrical characteristics acquired at elevated temperatures.

II. EXPERIMENTAL DETAILS

The EG films were grown on the Si-face of commercial semi-insulating 4H-SiC substrates[12] with zero off-cut angle and resistivity of $>10^9$ Ω·cm. The wafers were diced into $7 \times 7\,mm^2$ pieces and the EG growth process was performed in an upgraded commercial rapid thermal processor[13] with background pressure of $<2 \times 10^{-6}$ Torr. The furnace utilized RF inductive heating of a graphite susceptor and allowed for controlled heating and cooling of the samples with ramp rates up to 15 and 10 °C/s, respectively. An *in-situ* SiC wafer surface preparation step was performed by etching in 5% H_2/Ar forming gas at atmospheric pressure and a temperature of 1550 °C for 4 min. Prior to the EG growth, the substrates were subjected to a heating step at 1200 °C for 20 min. in high vacuum to reconstruct the SiC surface. Bilayer EG films were then grown at 1775 °C under high vacuum (2×10^{-5} Torr at growth temperature) for 60 min. The EG films grown were characterized by Raman spectroscopy using a Horiba Yvon LabRam HR system utilizing a 514.5 nm laser with a 700 nm spot size. The surface morphology was probed by Atomic Force Microscopy (AFM) using a Park Systems XE-150 operated in non-contact mode, as well as by Scanning Tunnelling Microscopy (STM) in an Omicron VT-SPM system operating in UHV conditions with a base pressure of 5×10^{-10} mbar. The full details of this EG growth process and EG material characterization are given elsewhere.[14]

To fabricate top-gated GFETs and test devices, patterning of the EG films was first performed by using reactive ion etching (RIE) in an oxygen plasma with an Al mask. This was followed by Al mask removal in AZ-326 MIF developer and rinsing in deionised water. After that, a 3 nm thick Al layer was deposited by e-beam evaporation and left to oxidize naturally in air in order to act as a seeding layer required to obtain uniform ALD growth of Al_2O_3 on the chemically inert and hydrophobic graphene.[15] An Al_2O_3 film was deposited by ALD in an Oxford Instruments Flex Al reactor with trimethyl aluminium and water vapour used as precursors. The growth process was performed at 120 °C and chamber pressure of 80 mTorr. A film thickness of 27 nm was measured by spectroscopic ellipsometry. After that, the gate dielectric was patterned by etching in buffered HF and Ti(10 nm)/Au(50 nm) ohmic contacts and gate electrodes were deposited by e-beam evaporation and patterned by the lift-off procedure. The GFETs had a gate length (L_G) of 4 μm, a gate width (W) of 30 μm and a source-drain distance of 30 μm. Test structures for measurements of contact resistivity (ρ_c) and EG sheet resistance (R_{sh}) by the Transfer Length Method (TLM)[16] had graphene with no gate dielectric, ohmic contact pads of 40 μm width and pad separations varying between 3 μm and 12 μm. Test structures for Hall measurements had van der Pauw geometry with $30 \times 30\,\mu m^2$ graphene squares with no gate dielectric stack. All electrical characterisations were performed on-wafer in a temperature-controlled environment. Electrical characterization of the GFETs and TLM structures was performed using an Agilent 4155C parameter analyser. GFETs gate capacitance was measured by a Keithley 4200-SCS semiconductor characterization system at 30 mV/100 kHz test signal. Hall measurements were performed with a computer controlled magnetic field changing from −0.2 to 0.2 T, electric field strength below 50 V/cm and a dissipated power density below 0.6 W/cm^2.

III. EXPERIMENTAL RESULTS AND DISCUSSION

A. Characterisation of epitaxial graphene grown on 4H-SiC

The number of monolayers (ML) in grown EG films was first estimated by micro Raman spectroscopy. Figure 1 shows 2D bands of bilayer EG and, for comparison, of monolayer EG. Monolayer graphene has a 2D peak at around 2720 cm^{-1}, which can be fitted with a single Lorentzian function (shown by solid line in Fig. 1(b)). A 2D band of bilayer EG (Fig. 1(a)) is shifted towards higher wave numbers compared with that of monolayer graphene. It has an asymmetrical shape with higher low-frequency shoulder and its fitting requires a sum of Lorentzian components. This is a clear signature of Bernal stacked layer,[17,18] which is typical for few layer graphene films grown by sublimation on the Si-face of SiC substrates.[19] The split of the four peaks fitting the 2D band of bilayer graphene is −33; −9; 8; and 30 cm^{-1} which compares well with theoretical values of −44; −11; 11; and 41 cm^{-1} calculated for 514.5 nm excitation.[17] In all cases, the full width at half maximum of the 2D Raman band ($FWHM_{2D}$) and its position (P_{2D}) were consistent with previously determined empirical dependencies of $FWHM_{2D}$ and P_{2D} on the layer number for EG grown on the Si-face of SiC.[20] A $FWHM_{2D}$ corresponding to 2–3 ML EG (65–85 cm^{-1}) was measured on EG films grown at 1775 °C for 60 min. The growth process was found to be self-limiting, with longer growth runs (up to 90 min. tested) having no further effect on the $FWHM_{2D}$ value. This occurred as a result of the already-grown graphene layers acting as a diffusion barrier to Si, hindering any further silicon desorption from the SiC surface.[21] The Raman spectra were

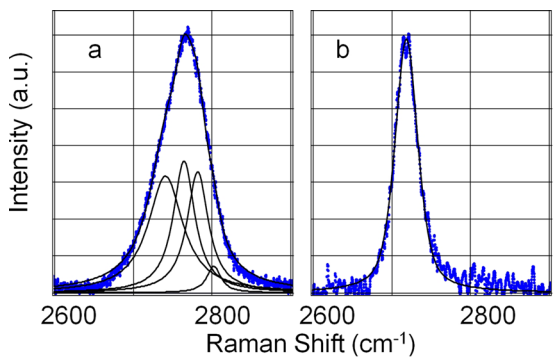

FIG. 1. 2D bands in Raman spectra of (a) bilayer EG grown at 1775 °C for 60 min in high vacuum ($P_{2D} = 2767\,cm^{-1}$; $FWHM_{2D} = 68\,cm^{-1}$); and (b) monolayer EG grown at 1800 °C for 4 min in high vacuum ($P_{2D} = 2724\,cm^{-1}$; $FWHM_{2D} = 32\,cm^{-1}$).

reproducible over the entire SiC substrates and from sample to sample.

To confirm the thickness of the EG films grown with these process parameters, test EG films were grown under the same regimes on conductive n-type 4H-SiC substrates and characterized by STM. Figure 2(a) shows an STM scan of five atomically flat SiC terraces covered by the graphene film. The SiC steps between terraces are discernible by the large colour contrast. Lower contrast change corresponds to the steps in graphene films. Line profiles over these low contrast boundaries give a step height of 3.35 Å corresponding to the spacing between graphene layers. The net of bright lines, clearly seen in the image, corresponds to wrinkles (or pleats) in the EG film caused by thermal strain release in graphene during sample cooling.[22] They cross both graphene terraces and steps in the SiC substrate, indicating that the graphene film is continuous across the entire surface and is at least partially bilayer. It is worthwhile to note that wrinkles clearly adhere at SiC terrace edges resulting in considerable anisotropy of graphene domain sizes along and across the SiC steps. The same wrinkle adherence to steps in the SiC substrate is clearly seen in the AFM scan shown in Figure 3. Observation of such wrinkle adherence by two different methods confirms that it is a result of the graphene growth (cooling) process and not caused by the measurements, e.g., by dragging wrinkles with the STM tip. The atomic-scale STM scan, shown in Figure 2(b), confirms the formation of a regular hexagonal graphene lattice over the SiC surface, as well as the formation of a buffer layer with a $(6\sqrt{3}\times 6\sqrt{3})R30^{\circ}$ surface reconstruction, as is expected for epitaxial graphene grown on the Si-face of SiC substrates.[23] The clear observation of surface reconstruction gives an upper bound of 3 ML for the graphene thickness since it is barely visible in thicker films. Another indirect estimation of the number of layers in the graphene films grown is provided by Hall measurements. Figure 4 shows Hall mobilities depending on charge carrier density measured at 22 °C (RT) in EG films grown on the Si-face of 4H-SiC in high vacuum at 1775 °C for 60 min and at 1800 °C for 4 min. All samples demonstrated n-type conductivity and had electron mobility values consistent with the literature data for graphene grown on the Si-face of 4H-SiC substrates,[24] shown by open triangles in Fig. 4. The EG films grown at 1775 °C for 60 min and

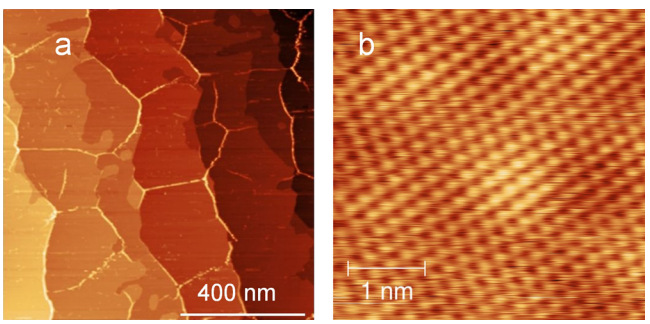

FIG. 2. STM images of EG films grown at 1775 °C for 60 min on the Si-face of a SiC on-axis substrate: (a) large-area scan taken at imaging conditions of V = 2.2 V and $I = 300$ pA; and (b) atomic-scale scan taken at imaging conditions of $V = 200$ mV and $I = 2.00$ nA.

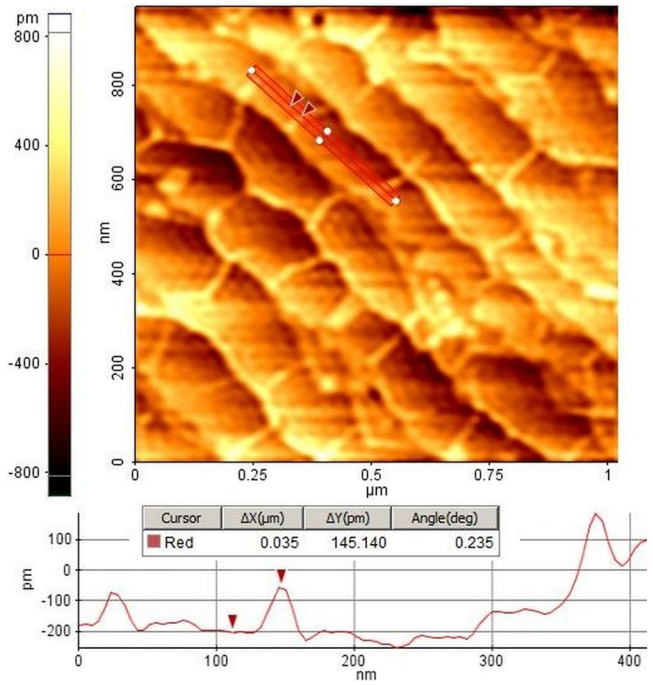

FIG. 3. 1×1 μm AFM scan of EG grown at 1775 °C for 60 min on the Si-face of 4H-SiC. The bottom panel shows a line section across the graphene wrinkles.

corresponding to 2–3 ML graphene by $FWHM_{2D}$ have electron densities (n_e) exceeding 6×10^{12} cm^{-2} and are clearly distinguishable from the EG films grown at 1800 °C for 4 min, which have $n_e < 3 \times 10^{12}$ cm^{-2} and $FWHM_{2D}$ corresponding to 1 ML graphene. Based on all these material characterizations, it was concluded that the EG films grown at 1775 °C for 60 min were continuous and primarily 2 ML thick. These EG films were then selected and used for GFET fabrication.

B. Electrical characterization of top gated bilayer GFETs

Figure 5 shows that the fabricated GFETs were capable of room temperature operation at drain current densities (I_D) up to 180 mA/mm with gate current densities (I_G) remaining

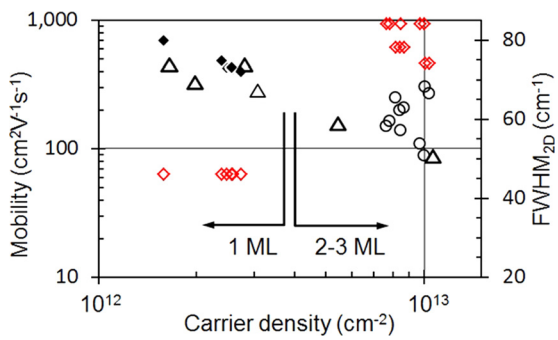

FIG. 4. Hall mobilities as a function of charge carrier density measured at RT in EG films grown on the Si-face of 4H-SiC in high vacuum at 1775 °C for 60 min (open circles) and at 1800 °C for 4 min (solid diamonds). Triangles denote the literature data[22] for Hall mobility in graphene grown on the Si-face of 4H-SiC. Open diamonds show $FWHM_{2D}$ dependence on the charge carrier density in the same samples.

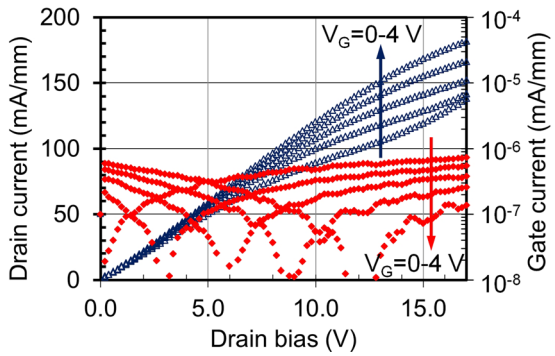

FIG. 5. I_D-V_D (triangles) and I_G-V_D (diamonds) characteristics of a top-gated bilayer GFET measured at RT with V_G as a parameter changing from 0 to 4 V.

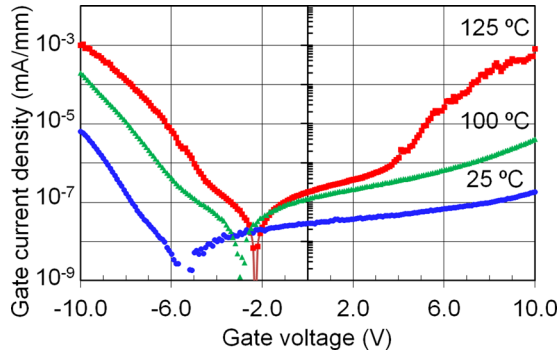

FIG. 7. Gate leakage current density dependence on the gate voltage in a top-gated GFET measured at different temperatures. The ALD-deposited Al_2O_3 gate dielectric layer is 27 nm thick.

below 10^{-6} mA/mm. The GFETs operated in the linear region at all applied drain voltages (V_D) and demonstrated I_D modulation as a function of the applied gate voltage (V_G). The GFETs did not close completely since the gate area in fabricated devices was much larger than the average domain size in the EG films, leading to the existence of "electron-hole puddles" in graphene[25] and non-zero conductivity at V_{CNP}. Nevertheless, the Dirac point was clearly observed in the g_m-V_G characteristics shown in Figure 6 as a gate voltage where g_m changes sign from negative (hole channel conductivity) to positive (electron channel conductivity). The V_{CNP} voltage increased following the applied drain voltage with $\Delta V_{CNP} \approx 0.5 \Delta V_D$ due to high source-gate (R_{SG}) and drain-gate (R_{DG}) access resistances in the fabricated devices and their symmetrical geometry ($R_{SD} = R_{SG} = R$). The peak measured transconductance increased with applied V_D, consistent with the expression given for a long-channel FET in its linear working region[10]

$$g_m = \mu \frac{C_G}{L_G} V_D, \tag{1}$$

where C_G is the gate capacitance per unit area, and μ is the carrier mobility. The g_m/V_D ratio was measured up to 0.45 mS/mm/V in the best devices fabricated.

Figure 7 shows the dependence of gate leakage current density on applied V_G at elevated temperatures in the fabricated GFETs, measured to evaluate its capacity for high temperature operation. I_G remained below 10^{-3} mA/mm at temperatures up to 125 °C and applied gate voltages up to 10 V, although excess gate current is clearly seen at this temperature and $|V_G| > 4$ V indicating the start of gate dielectric performance deterioration. At a temperature of 100 °C and below, the ALD-deposited Al_2O_3 gate dielectric remained stable and withstood gate voltages up to ±10 V corresponding to a dielectric strength exceeding 4.5 MV/cm. The leakage current density remained below 2×10^{-4} mA/mm (corresponding to 5×10^{-3} A/cm^2) at 100 °C. This value is comparable with those of other ALD grown Al_2O_3 films on SiC[26] and GaAs.[27] Figure 8 shows I_D-V_G and g_m-V_G characteristics of top-gated GFETs measured at temperatures up to 100 °C. Although the I_D on/off ratio is small due to the relatively low fraction of the gate-modulated channel length,[28] the Dirac charge neutrality point is clearly observed at all operating temperatures. V_{CNP} was found to shift to more positive voltages and the peak transconductance noticeably rose as the temperature was increased from 25 °C to 100 °C, as shown in Figure 9. The V_{CNP} change could potentially result

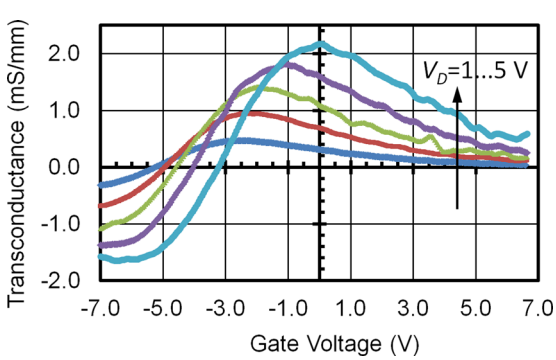

FIG. 6. g_m-V_G characteristics of a top-gated bilayer GFET measured at RT with V_D as a parameter changing from 1 to 5 V.

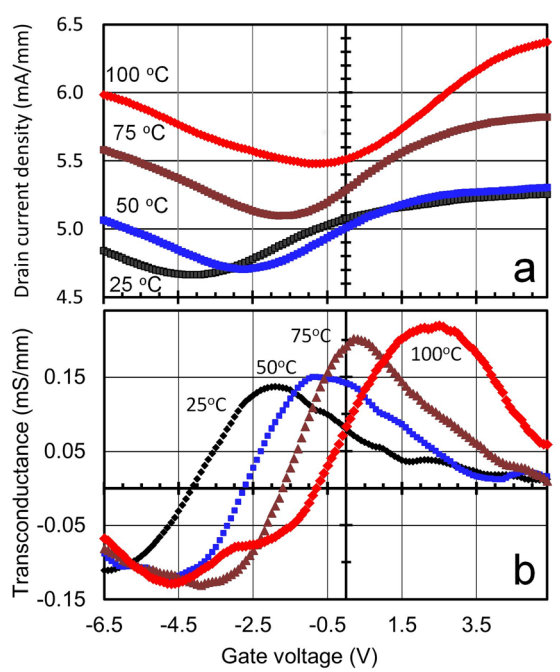

FIG. 8. (a) I_D-V_G and (b) g_m-V_G characteristics of a top-gated GFET measured at $V_D = 1.0$ V and operating temperatures up to 100 °C.

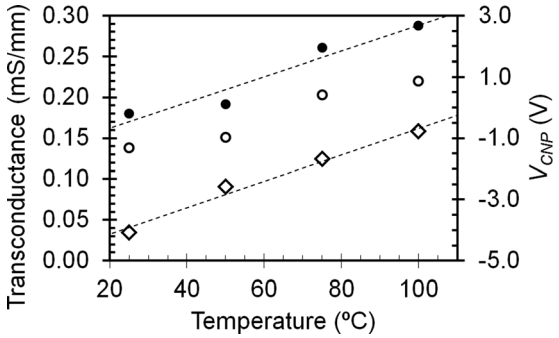

FIG. 9. The charge neutrality point voltage (open diamonds), measured (open circles) and intrinsic (open circles) peak transconductances as functions of the operating temperature of a top-gated GFET with 4 μm gate length measured at $V_D = 1.0$ V. Dotted linear trendlines are given as a guide to the eye.

from a number of causes since the position of the Dirac point in GFETs is a sensitive parameter which can be influenced by the work function of the gate metal,[29] chemical doping,[30] random charged impurities,[31] and the properties of the deposited gate dielectric layer.[32] For example, the work function difference that exists between titanium and graphene would be expected to exhibit some form of temperature dependence, which would act to affect the position of the Dirac point. Alternatively, operation of the devices at higher temperatures may also lead to the desorption of attached molecules like water from the exposed regions of the graphene channel, which could also result in shifting of the Dirac point. The rise of peak transconductance was expected in bilayer GFETs following Eq. (1), due to increase of charge carrier mobility in 2–3ML graphene,[8] but two parameters have to be excluded to confidently draw the conclusion that the increase of g_m is indeed defined by a change in mobility. First, Eq. (1) does not include the effect of the source-gate and drain-gate access resistances (R), which have a strong impact on the measured transconductance in GFETs[33] and depend on graphene-metal contact resistivity and the resistance of the graphene channel not covered by the gate. It has been demonstrated in previous studies that, for Ti/Au contacts deposited onto EG, both the contact resistivity and the graphene sheet resistance tend to decrease as the temperature increases.[34] To exclude this effect, the intrinsic transconductance (g_m^i) can be derived from the measured value by the following expression:[35]

$$g_m^i = \frac{g_m^0}{1 - 2Rg_d\left(1 + Rg_m^0\right)}, \tag{2}$$

where $g_m^0 = g_m/(1 - Rg_m)$; and g_d is the measured source-drain conductance. Temperature dependent measurements were performed to map ρ_c and R_{sh} values by TLM, with the results indicating a clear and significant reduction in both the contact resistivity and the sheet resistance with an increase in the device operating temperature, as shown in Figure 10. The intrinsic transconductance was then extracted by calculating the R value for each temperature and substituting R and the measured values of g_m into Eq. (2). The resultant peak intrinsic transconductance is shown by solid circles in

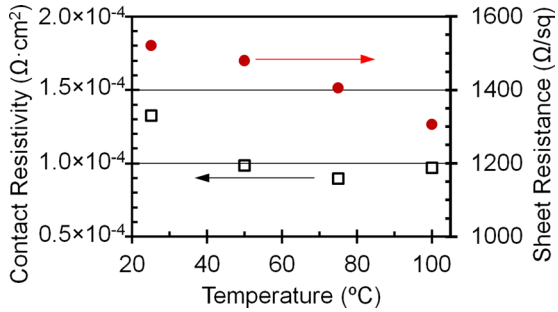

FIG. 10. The contact resistivity of Ti/Au ohmic contacts (squares) and sheet resistance of bilayer epitaxial graphene grown on the Si face of 4H-SiC extracted from TLM measurements at different temperatures.

Fig. 9, and still increases with temperature even after excluding the effect of access resistance.

The second parameter affecting the GFET transconductance in Eq. (1) is the gate capacitance which is the total capacitance of two capacitors connected in series, the gate oxide capacitor and quantum capacitor of the graphene channel. For the GFETs fabricated, a gate oxide capacitance per unit area of 0.3 μF/cm^2 was calculated using a relative permittivity of 9.0 for amorphous ALD-grown Al_2O_3.[24] The measured C_G values are shown in Figure 11 and were found to be dependent on the gate voltage as an effect of the quantum capacitance. Nevertheless, the relative change of the gate capacitance with temperature was found to be $(dC_G/dT)/C_G \sim 1.3 \times 10^{-3}$ °C^{-1}, while the relative change of the peak intrinsic transconductance was found to be significantly larger: $(dg_m^i/dT)/g_m^i \sim 9 \times 10^{-3}$ °C^{-1}. This leads us to the conclusion that the increase of GFET transconductance is caused mainly by the temperature dependence of the charge carrier mobility in bilayer epitaxial graphene.

IV. SUMMARY

Top-gated graphene FETs have been fabricated utilizing bilayer epitaxial graphene grown on the Si-face of 4H-SiC substrates by thermal decomposition of silicon carbide in high vacuum. Graphene films were characterized by Raman spectroscopy, AFM, STM and Hall measurements to estimate graphene thickness, morphology and charge transport properties. The graphene growth process was found to be self-limiting resulting in 2–3 monolayer thick graphene films. The as-grown graphene was found to be continuous

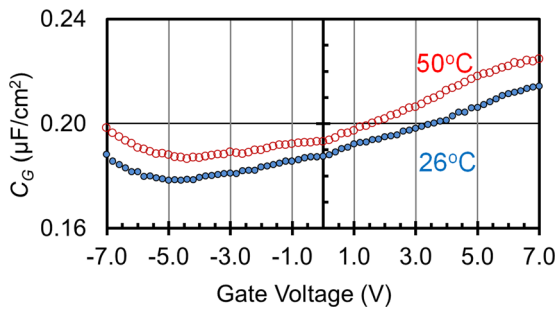

FIG. 11. The total gate capacitance in a top-gated bilayer GFET as a function of the gate voltage, measured at 26 °C (solid markers) and 50 °C (open markers).

across the entire substrate surface and separated by wrinkles into domains. Noticeable wrinkle adherence at SiC terrace edges resulting in considerable anisotropy of graphene domain sizes was observed by AFM and STM. A 27 nm thick Al_2O_3 was grown by atomic layer deposition with an e-beam evaporated Al seed layer to function as a gate oxide. The long-channel GFETs exhibited stable room temperature operation at drain current densities up to 180 mA/mm with gate current densities remaining below 10^{-6} mA/mm. The GFETs were able to operate at temperatures up to 100 °C, this upper limit imposed by deterioration of the gate dielectric performance at higher temperatures. The GFETs demonstrated a gate oxide dielectric strength exceeding 4.5 MV/cm and the leakage current density remained below 2×10^{-4} mA/mm (5×10^{-3} A/cm^2) at 100 °C. Significant shifting of the charge neutrality point and an increase of the peak transconductance were observed in the GFETs as the operating temperature was increased. The GFET transconductance change was apparently defined by the temperature dependence of the electron mobility in bilayer graphene. This sensitivity of the device characteristics to an elevated operating temperature has to be taken into account in the development of GFETs and the design of analogue circuits.

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